and second wiring patterns.

## REMARKS

The Office Action dated December 13, 2002 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 13 and 14 have been amended. New claims 16-19 have been added. No new matter has been added by the amendments made herein. Accordingly, claims 13, 14 and 16-19 are pending in the present application and are respectfully submitted for consideration.

The Office Action rejected claim 13-14 under 35 U.S.C. §103(e) as being unpatentable over Matsuoka (U.S. Patent 5,640,033) in view of Satoh et al. (U.S. Patent 5,375,069). The Office Action takes the position that Matsuoka and Satoh teach or suggest all the features recited in claims 13 and 14. Applicants respectfully disagree.

Claim 13 is directed to a method of manufacturing a semiconductor device for forming a first wiring pattern and second wiring pattern at the same time on a same level. The first wiring pattern is connected to a gate electrode on a gate insulating film formed on a semiconductor region, and the second wiring pattern is connected to the semiconductor region. In patterning of the first and second wiring pattern, a dummy wiring pattern is electrically separated from and placed between the first and second wiring patterns on the same level is left unetched, the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

The essence of the claimed invention as recited in claim 13 is a dummy wiring pattern electrically separated from and placed between the first and second wiring patterns on the same level is left unetched, and the dummy wiring pattern is not positively serving as any element in a circuit of the semiconductor device. The dummy wiring pattern is used for adjusting the spaces in the wiring patterns subjected to etching. The benefits provided by the claimed invention include pattern etching that is uniformized and having the micro loading effects of substantially the same degree. Thus, it is submitted that the applied references neither teach the features nor the benefits provided of the claimed invention.

Matsuoka is directed to a semiconductor device having a fine gate structure.

Specifically, Matsuoka discloses a method for forming a first wiring layer 51 and a second wiring layer 57. The first wiring layer 51 is electrically connected to a gate electrode 53 via a first contact portion 52. A source region is electrically connected the second wiring layer 57 via a second contact portion 56. A drain region 54b is electrically connected to a third wiring layer via a third contact portion. A third wiring layer 59 is electrically connected to a drain region 55a via a fourth contact portion 60. Thus, Matsouka discloses a first, second and third wiring patterns which are used as a gate, source, and drain electrodes. However, Matsuoka neither teaches nor suggests a dummy wiring pattern as recited in the claimed invention.

Satoh is directed to a wiring processing methods or wiring routes in semiconductor integrated circuits devices. More specifically, Satoh discloses wiring layers that are insulated mutually by inter-level films and wirings that are adjacent to the one another through the inter-level insulating films. The Office Action takes the position that Satoh discloses that spaces 23, 24, and 25 are among the third 16, first 14, and second 15 wiring layer are set generally equal to a minimum pattern space of the third, first, and second wiring layers. However, the wiring layers 14, 15, and 16 are multi-level wiring layers. In other words, the wiring layers are on different levels. Furthermore, Satoh fails to teach or suggest a dummy wiring pattern. Therefore, Satoh does not cure the deficiencies of Matsuoka. As a result, it is submitted that the combination of Matsuoka and Satoh neither teach nor suggest all the features recited in claims 13 and 14. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 13 and 14.

New claims 16-19 are added. It is submitted that new claims 16-19 also recite the feature of a dummy wiring pattern, which is neither taught nor suggested by the applied art. Accordingly, Applicants request the favorable consideration of new claims 16-19 for at least the reasons set forth above with respect to claims 13 and 14.

In view of the distinctions discussed above and the above amendments, withdrawal of the rejections to claims 13 and 14 is respectfully requested. Claims 13 and 14 are amended. Claims 16-19 are added. No new matter is presented. Accordingly, in view of the above remarks and amendments, Applicants submit that the application is now in condition for allowance and that this application be passed to issue.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number

listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

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Enclosure: Marked-up Copy of the Claims

MARKED-UP COPY OF CLAIMS

13. (Amended) A method of manufacturing a semiconductor device for forming a first wiring [layer] pattern and a second wiring [layer] pattern at the same time on a same level, said first wiring [layer] pattern being connected to a gate electrode on a gate insulating film formed on a semiconductor region, and said second wiring [layer] pattern being connected to said semiconductor region, wherein in patterning said first and second wiring [layer] patterns, a [third] dummy wiring [layer] pattern electrically separated from and placed between said first and second wiring [layers] patterns on said same level is left unetched, the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

14. (Amended) A method according to claim 13, wherein the spaces [among] between said dummy pattern and said [third] first, and second wiring [layers] patterns are set generally equal to a minimum pattern space of said [third] first, and second wiring [layers] patterns.